hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.--

A1 cont.

Please replace the paragraph beginning on page 4, line 6, with the following rewritten paragraph:

--The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:--

A2

IN THE CLAIMS:

Please cancel claims 1-4 without prejudice or disclaimer of the subject matter contained therein.

Please amend the claims as follows:

A3

5. (Amended) An ESD protection component, comprising:

Sub B1

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

A3 Cont.

a first doping area of the second conductivity type, formed in the connecting area;

wherein each of the MOS FETs has a source region of the first conductivity type, coupled to a power rail.

6. (Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein the first well is coupled to a pad through the extension areas.

7. (Amended) An ESD protection component, comprising:

A3 Cont.

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein the first doping region is coupled to a pad.

8. (Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein each of the MOS FETs has a drain region of the first conductivity type, coupled to a pad.

A3 Cont.

9. (Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, comprising:

two gates, formed in parallel on a first semiconductive layer having a second conductivity type;

two sources of the first conductivity type, coupled to a power supply; and

two drains of the first conductivity type;

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

A3

a first doping area of the second conductivity type, formed in the connecting area, and coupled to a pad; and

a guard ring of the second conductivity type, formed on the first semiconductive layer, coupled to the power supply;

wherein the first well is coupled to the pad through the extension areas.